This work is concerned with the use of algebraic methods to model – and optimise the use of - asynchronous processes in the design of digital hardware. The talk will focus particularly on a technique known as `time stealing' whereby the use of a multiphase clock can allow for a more flexible use of time. In this approach the system is clocked periodically, but within each clock cycle processes are allowed to interact asynchronously. Thus, longer processes can be juxtaposed with shorter processes---they can `steal time' from the shorter processes---to allow the use of shorter clock periods than would otherwise be possible. As far as we are aware, time stealing designs are generally accomplished using heuristic methods. Indeed, the lack of a simple algorithmic approach to time stealing has led to it falling into disuse in favour of more conservative, but algorithmic, design principles. Here, we wish to show that there exists a mathematically rigorous approach to this problem. In fact, we will show that the problem reduces to one of solving a linear equation over the max-plus semi-ring. `Max-plus algebra' was originally championed by Cunningham-Greene and has applications in queueing theory and even railway time tabling. An attempt will be made, however, to ensure that this talk is self-contained.